UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/815,903	03/31/2004	Debendra Das Sharma	42P18579	9298

8791 7590 03/31/2008

BLAKELY SOKOLOFF TAYLOR & ZAFMAN
1279 OAKMEAD PARKWAY
SUNNYVALE, CA 94085-4040

EXAMINER	
BAE, JI H	

ART UNIT	PAPER NUMBER
2115	

MAIL DATE	DELIVERY MODE
03/31/2008	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/815,903	SHARMA ET AL.	
	Examiner	Art Unit	
	JI H. BAE	2115	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *31 March 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-29* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-29* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 1-29 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Chip verification is generally known in the art as a way to test the functional behavior of a design in response to various test stimuli. Since verification typically refers to the "pre-hardware" testing of a design, it is normally carried out entirely via software simulations of hardware models. For example, a testbench is written to test various features of a RTL description of a design, often in Verilog or VHDL. The testbench and verification environment are compiled and simulated with various test vectors, with results examined to determine whether any errors exist in the design.

Applicant's specification is directed towards a verification strategy for asynchronous links. From the disclosure, it is clear that applicant's verification strategy is intended to be carried out via simulation within a computing environment. This can be observed in Fig. 1, which shows that bus functional models are being used to interface between the verification environment and the chip under test. As is known in the art, bus functional models are software models that take the place of actual system components in the verification environment.

However, applicant’s claims do not make this distinction clear. A plain reading of the claims would suggest that the invention comprises actual hardware devices and/or methods of using actual hardware devices, when in fact applicant's invention is a simulation of actual hardware devices. In particular, the claims to an apparatus, system, and article of manufacture

are misleading because the elements of the claimed apparatus/system/article are not actual devices but rather software models. The only element of the invention which would correctly be claimed as an apparatus or article of manufacture would be the computer system that executes the simulation.

Claim Rejections - 35 USC § 103

Claims 1, 2, 5, 6, and 21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Komatsu et al., U.S. Patent No. 7,007,212, in view of Knaack, U.S. Patent No. 6,023,777.

Regarding claim 1, Komatsu teaches a method comprising:

receiving an input clock frequency [Fig. 1, CK at line 131, input to FIFO 113] and test data [Din, line 132, from tester 200] received at an input data frequency corresponding to the input clock frequency [col. 8, lines 64-66, FIFO 113 stores data at a rate determined by CK];

retaining a portion of the test data received in a first data buffer [FIFO 113];

shifting the input clock frequency to an output clock frequency [PLL 111 receives CK and outputs CKp1, which is sent to FIFO 113];

transmitting test data retained in the first data buffer to a second data buffer [FIFO 125] of a chip [DUT 100b] that supports asynchronous communications, wherein transmitting occurs at an output data frequency corresponding to the output clock frequency [col. 8, lines 66-67, FIFO 113, outputs data at a rate determined by CKp1].

Komatsu does not teach that the output clock frequency is varied over a period of time.

Knaack teaches a method for testing FIFOs with status flags, wherein a "shmoo" test is carried out for the read and write clocks [col. 4, lines 27-58].

It would have been obvious to one of ordinary skill in the art to combine the teachings of Komatsu with Knaack. Komatsu teaches a test system comprised of multiple FIFOs, but does

not teach that the FIFOs possess status flags. Status flags such as those suggested by Knaack are well-known in the art for providing an indication of a FIFO's capacity [Knaack, col. 1, lines 13-16]. It would have been obvious to one of ordinary skill in the art to combine the status flags taught by Knaack with the FIFOs taught by Komatsu. The operation of the FIFO status flags is generally known in the art, and would have provided the same functionality in the FIFOs of Komatsu. Thus, the combination of Knaack with Komatsu would have combined two known elements to yield a predictable result. Additionally, it would have been further obvious to apply the testing methods of Knaack with the combined system of Knaack/Komatsu. The testing method taught by Knaack is a method for testing FIFO status flags that represents an improvement over prior art methods [col. 2, lines 15-28]. Since the combination of Knaack/Komatsu includes the status flags taught by Knaack in the system of Komatsu, it would have been obvious to one of ordinary art to apply the teachings of Knaack regarding testing to the combination as well. The testing method would have provided the same functionality as disclosed by Knaack, and would therefore have combined known elements to yield predictable results.

Regarding claim 2, Komatsu teaches that the output data frequency is a frequency of the test data retained in the first data bugger transmitted at the output clock frequency [col. 8, lines 66-67, FIFO 113, outputs data at a rate determined by CKp1].

Regarding claim 5, Knaack teaches varying the output clock frequency between a maximum and a minimum [col. 4, lines 27-32, write clock ahead of read clock by 4ns and the difference is gradually decreased].

Regarding claim 6, Knaack teaches varying the output clock frequency during a period of time depending on the input data frequency [col. 4, lines 27-32, shmoo test varies the difference between the clocks].

Regarding claim 21, Komatsu/Knaack teaches the method of claim 1, and also the system to execute the claimed method.

Claims 4, 10, 13, and 24 are rejected under 35 U.S.C. 103(a) as being unpatentable over Komatsu and Knaack as applied to claim 1 above, and further in view of Chang et al., U.S. Patent No. 6,347,380.

Komatsu/Knaack teaches the method of claim 1, but does not teach an upper/lower watermark that determines the output clock frequency setting.

Chang teaches a method for adjusting the clock for a FIFO read pointer according to an upper/lower watermark [Fig. 6, TL1, BL1, col. 8, lines 28-60].

It would have been obvious to one of ordinary skill in the art to combine the teachings of Chang with Komatsu/Knaack. Komatsu/Knaack teaches a test system comprised of FIFOs which are used for transmitting/receiving the test data, while Chang is directed towards a method for preventing FIFO underflow/overflow conditions. Chang's teachings of a method to prevent FIFO underflow/overflow conditions could have been combined with the system taught by Komatsu/Knaack. In the combination with Komatsu/Knaack, the method of Chang would have provided the same functionality as that originally disclosed by Chang. Thus, the combination of Chang with Komatsu/Knaack would have combined known elements to yield predictable results.

Regarding claim 10, Chang teaches varying the output clock frequency to maintain the data in first buffer between the upper and lower watermark.

Regarding claims 13 and 24, Komatsu/Knaack/Chang teaches the method of claim 4, and also the apparatus and article of manufacture with instructions to execute the claimed method.

Claim 27 is rejected under 35 U.S.C. 103(a) as being unpatentable over Komatsu/Knaack as applied to claim 1 above, and further in view of LeColst, U.S. Patent No. 6,476,628.

Regarding claim 27, Komatsu/Knaack teaches a system as claimed in claim 27, but does not teach a second chip, frequency modifier, and elastic data buffer.

LeColst teaches that semiconductor testers often employ parallel architectures, wherein multiple DUTs are tested in parallel [Fig. 1, col. 1, lines 23-36].

It would have been obvious to one of ordinary skill in the art to combine the teachings of LeColst with Komatsu/Knaack. Komatsu/Knaack teaches a test system for semiconductor devices, but does not teach parallel testing of DUTs. LeColst teaches that parallel testing improves throughput of the manufacturing process and reduces overall costs [col. 1, lines 34-36]. Therefore, it would have been obvious to apply the teaching regarding parallel test to the combination of Komatsu/Knaack. The teachings of LeColst would improve the system of Komatsu/Knaack by providing the increased manufacturing throughput and reduced cost, as disclosed.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure:

Smith, U.S. Patent No. 6,584,584,

Sandoval, U.S. Patent No. 6,990,073,

Wiggins, U.S. Patent No. 6,519,722,

Haass et al., U.S. Patent No. 6,876,207,

Toshitani, U.S. Patent No. 7,042,911,

Ozawa, U.S. Patent Application Publication No. 2004/0022099,

Sindalovsky, U.S. Patent No. 6,745,265,

Virzi, U.S. Patent No. 5,953,372.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to JI H. BAE whose telephone number is (571)272-7181. The examiner can normally be reached on Monday-Friday, 10 am to 6:30 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Thomas Lee can be reached on 571-272-3667. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Ji H. Bae
Patent Examiner
Art Unit 2115
U.S. Patent and Trademark Office
571-272-7181
ji.bae@uspto.gov

/Thomas Lee/

Supervisory Patent Examiner, Art Unit 2115